What is claimed is:

1    1.    An inductor in an integrated circuit, comprising:

2         a conductive trace disposed over an insulating layer, said insulating layer overlying a

3    semiconductor substrate of a first conductivity type; and

4         at least two deep wells of opposite conductivity type in said substrate underneath said

5         track.

1    2.    The inductor of claim 1 wherein said conductive trace comprises metal.

1    3.    The inductor of claim 1 wherein said semiconductor substrate is a p-type substrate and

2    said deep wells are n-type wells

1    4.    The inductor of claim 1 wherein said semiconductor substrate is an n-type substrate and

2    said deep wells are p-type wells.

1    5.    The inductor of claim 1 wherein said deep wells are not reverse biased.

1    6.    The inductor of claim 1 wherein said deep wells are arranged in a pattern to form a

2    substantial depletion space in said substrate underneath said trace.

1    7.    The inductor of claim 1 wherein said deep wells are cuboid.

1    8.    The inductor of claim 1 wherein said deep wells are L shaped cuboid.

1    9.    The inductor of claim 1 wherein said deep wells are continuous.

1    10.   The inductor of claim 9 wherein said deep wells are continuous for at least 1.5 $\mu$m

2    approximately from a surface of said substrate underneath said insulating layer.

1    11.   The inductor of claim 1 wherein said deep wells are formed by ion implantation.

1   12.   The inductor of claim 11 wherein said ion implantation comprises a first stage in which

2   ions are accelerated to a first energy level and at least a second stage in which ions are

3   accelerated to an energy level different from said first energy level.


1   13.   An inductor in an integrated circuit, comprising:

2         a conductive trace disposed over an insulating layer, said insulating layer overlying a

3   semiconductor substrate of a first conductivity type;

4         a shallow trench isolation region, formed in said substrate underneath said trace; and

5         at least two deep wells of opposite conductivity type in said substrate underneath said

6   shallow trench isolation region.


1   14.   The inductor of claim 13 wherein said conductive trace comprises metal.


1   15.   The inductor of claim 13 wherein said shallow trench isolation comprises silicon dioxide.


1   16.   The inductor of claim 13 wherein said semiconductor substrate is a p-type substrate and

2   said deep wells are n-type wells.


1   17.   The inductor of claim 13 wherein said semiconductor substrate is an n-type substrate and

2   said deep wells are p-type wells.


1   18.   The inductor of claim 13 wherein said deep wells are not reverse biased.


1   19.   The inductor of claim 13 wherein said deep wells are arranged in a pattern to form a

2   substantial depletion space in said substrate underneath said trace.


1   20.   The inductor of claim 13 wherein said deep wells are cuboid.


1   21.   The inductor of claim 13 wherein said deep wells are L shaped cuboid.


1   22.   The inductor of claim 13 wherein said deep wells are continuous.

1   23.   The inductor of claim 22 wherein said deep wells are continuous for at least 1.5 μm
2   approximately from a plane in said substrate underneath and adjacent to said shallow trench
3   isolation region.

1   24.   The inductor of claim 13 wherein said deep wells are formed by ion implantation.

1   25.   The inductor of claim 24 wherein said ion implantation comprises a first stage in which
2   ions are accelerated to a first energy level and at least a second stage in which ions are
3   accelerated to an energy level different from said first energy level.

1   26.   A method of manufacturing an inductor on an integrated circuit, comprising:
2         providing a semiconductor substrate of a first conductivity type;
3         forming at least two deep wells of opposite conductivity type in said substrate;
4         forming an insulation layer over said substrate; and
5         forming a conductive trace over said insulating layer.

1   27.   The method of claim 26 wherein said deep wells are arranged in a pattern to form a
2   substantial depletion space in said substrate underneath said trace.

1   28.   The method of claim 26 wherein said deep wells are formed to be continuous.

1   29.   The method of claim 28 wherein said deep wells are continuous for at least 1.5 μm
2   approximately from a surface of said substrate underneath said insulating layer.

1   30.   The method of claim 26 wherein said deep wells are formed by ion implantation.

1   31.   The method of claim 30 wherein said ion implantation comprises a first stage in which
2   ions are accelerated to a first energy level and at least a second stage in which ions are
3   accelerated to an energy level different from said first energy level.

1    32.   The method of claim 31 wherein said first energy level in said first stage ranges

2    approximately from 500 to 800 Kev and said second energy level in said second stage ranges

3    approximately from 200 to 350 Kev.

1    33.   The method of claim 31 wherein said first energy level in said first stage ranges

2    approximately from 600 to 1200 Kev; said second energy level in said second stage ranges

3    approximately from 350 to 500 Kev; and a third energy level in a third stage ranges

4    approximately from 150 to 250 Kev

1    34.   A method of manufacturing an inductor on an integrated circuit, comprising:

2        providing a semiconductor substrate of a first conductivity type;

3        forming a shallow trench isolation region in a substrate;

4        forming at least two deep wells of opposite conductivity type in said substrate underneath

5    said shallow trench isolation region;

6        forming an insulation layer over said substrate; and

7        forming a conductive trace over said insulating layer.

1    35.   The method of claim 34 wherein said deep wells are arranged in a pattern to form a

2    substantial depletion space in said substrate underneath said trace.

1    36.   The method of claim 34 wherein said deep wells are formed to be continuous.

1    37.   The method of claim 36 wherein said deep wells are continuous for at least 1.5 μm

2    approximately from a plane in said substrate underneath and adjacent to said shallow trench

3    isolation region.

1    38.   The method of claim 34 wherein said deep wells are formed by ion implantation.

1    39.   The method of claim 38 wherein said ion implantation comprises a first stage in which

2    ions are accelerated to a first energy level and at least a second stage in which ions are

3    accelerated to an energy level different from said first energy level.

1    40.    The method of claim 39 wherein said first energy level of said first stage ranges

2    approximately from 500 to 800 Kev and said second energy level of said second stage ranges

3    approximately from 200 to 350 Kev.


1    41.    The method of claim 39 wherein said first energy level of said first stage ranges

2    approximately from 600 to 1200 Kev; said second energy level of said second stage ranges

3    approximately from 350 to 500 Kev, and a third energy level of a third stage ranges

4    approximately from 150 to 250 Kev.

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